1.0 Features

- Can be used in designs presently using the SYM20C15
- Single-chip, half-duplex 1200 bits per second FSK modem
- Bell 202 shift frequencies of 1200Hz and 2200Hz
- 3.3V - 5.0V power supply
- Transmit-signal wave shaping
- Receive band-pass filter
- Low power: optimal for intrinsically safe applications
- CMOS compatible
- Internal oscillator requires 460.8kHz crystal or ceramic resonator
- Meets HART physical layer requirements
- Industrial temperature range of -40°C to +85°C
- Available in 28-pin PLCC and 32-pin LQFP packages

2.0 Description

The A5191HRT is a single-chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit-signal shaping. The A5191HRT is pin-compatible with the SYM20C15. See the Pin Description and Functional Description sections for details on pin compatibility with the SYM20C15.

The A5191HRT uses phase continuous frequency shift keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half-duplex operation used in HART communications.

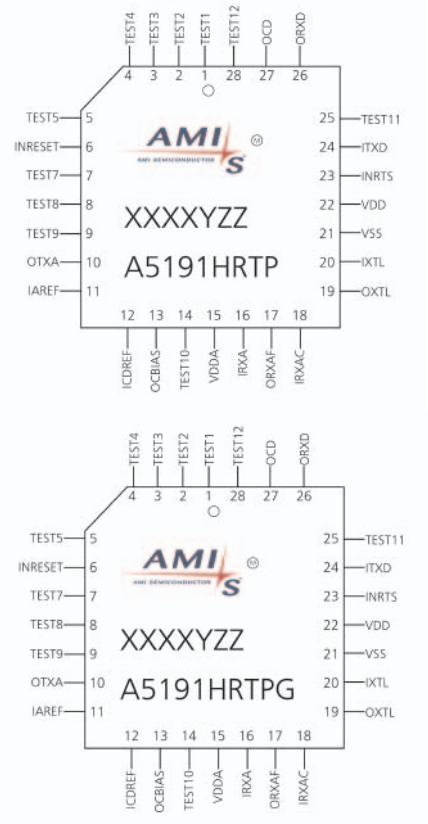


Figure 1: 28-Pin PLCC Pinout Diagrams (green & non-green)

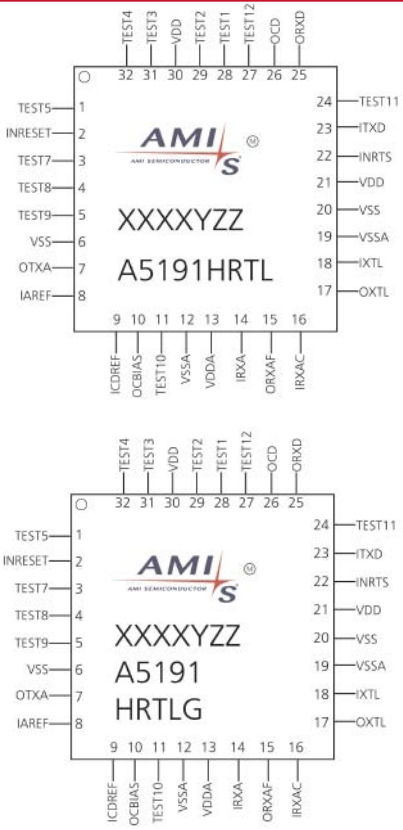


Figure 2: 32-Pin LQFP Pinout Diagrams (green & non-green)

Table 1: Pinout Summary 28-Pin PLCC, A5191HRTP/Pg (12197-504/508)

Pin No.	Signal Name	Type	Pin Description
1	TEST1	Input	Connect to V_{SS}
2	TEST2	-	No connect
3	TEST3	-	No connect
4	TEST4	-	No connect
5	TEST5	Input	Connect to V_{SS}
6	INRESET	Input	Reset all digital logic when low
7	TEST7	Input	Connect to V_{SS}
8	TEST8	Input	Connect to V_{SS}
9	TEST9	Input	Connect to V_{SS}
10	OTXA	Output	Output transmit analog, FSK modulated HART transmit signal to 4-20mA loop interface circuit
11	IAREF	Input	Analog reference voltage
12	ICDREF	Input	Carrier detect reference voltage
13	OCBIAS	Output	Comparator bias current
14	TEST10	Input	Connect to V_{SS}
15	VDDA	Power	Analog supply voltage
16	IRXA	Input	FSK modulated HART receive signal from 4-20mA loop interface circuit
17	ORXAF	Output	Analog receive filter output
18	IRXAC	Input	Analog receive comparator input
19	OXTL	Output	Crystal oscillator output
20	IXTL	Input	Crystal oscillator input
21	VSS	Ground	Ground
22	VDD	Power	Digital supply voltage
23	INRTS	Input	Request to sent
24	ITXD	Input	Input transmit date, transmitted HART data stream from UART
25	TEST11	-	No connect
26	ORXD	Output	Received demodulated HART data to UART
27	OCD	Output	Carrier detect output
28	TEST12	-	No connect

Table 2: Pinout Summary 32-Pin LQFP, A5191HRTL/Lg (12197-503/507)

Pin No.	Signal Name	Type	Pin Description
1	TEST5	Input	Connect to V_{SS}
2	INRESET	Input	Reset all digital logic when low, connect to V_{DD} for normal operation
3	TEST7	Input	Connect to V_{SS}
4	TEST8	Input	Connect to V_{SS}
5	TEST9	Input	Connect to V_{SS}
6	VSS	Ground	Digital ground
7	OTXA	Output	Output transmit analog, FSK modulated HART transmit signal to 4-20mA loop interface circuit
8	IAREF	Input	Analog reference voltage
9	ICDREF	Input	Carrier detect reference voltage
10	OCBIAS	Output	Comparator bias current
11	TEST10	Input	Connect to V_{SS}
12	VSSA	Ground	Analog ground
13	VDDA	Power	Analog supply voltage
14	IRXA	Input	FSK modulated HART receive signal from 4-20mA loop interface circuit
15	ORXAF	Output	Analog receive filter output
16	IRXAC	Input	Analog receive comparator input
17	OXTL	Output	Crystal oscillator output
18	IXTL	Input	Crystal oscillator input
19	VSSA	Ground	Analog ground
20	VSS	Ground	Digital ground
21	VDD	Power	Digital supply voltage
22	INRTS	Input	Request to send
23	ITXD	Input	Input transmit data, transmitted HART data stream from UART
24	TEST11	-	No connect
25	ORXD	Output	Received demodulated HART data to UART
26	OCD	Output	Carrier detect output
27	TEST12	-	No connect
28	TEST1	Input	Connect to V_{SS}
29	TEST2	-	No connect
30	VDD	Power	Digital supply voltage
31	TEST3	-	No connect
32	TEST4	-	No connect

3.0 Pin Descriptions

Table 3: Pin Descriptions

Symbol	Pin Name	Description
IAREF	Analog Reference Voltage	Analog input sets the dc operating point of the operational amplifiers and comparators and is usually selected to split the dc potential between V_{DD} and V_{SS}. See IAREF in DC Characteristics, Table 6
ICDREF	Carrier Detect Reference Voltage	Analog input controls at which level the carrier detect (OCD) becomes active. This is determined by the dc voltage difference between ICDREF and IAREF. Selecting ICDREF - IAREF equal to 0.08 V_{DC} will set the carrier detect to a nominal 100 mV_{p-p}
INRESET	Reset Digital Logic	When at logic low (V_{SS}) this input holds all the digital logic in reset. During normal operation INRESET should be at V_{DD}. INRESET should be held low for a minimum of 10nS after V_{DD} = 2.5V as shown in Figure 3
INRTS	Request to Send	Active-low input selects the operation of the modulator. OTXA is enabled when this signal is low. This signal must be held high during power-up
IRXA	Analog Receive Input	Input accepts the 1200/2200Hz signals from the external filter
IRXAC	Analog Receive Comparator Input	Positive input of the carrier detect comparator and the receiver filter comparator
ITXD	Digital Transmit Input (CMOS)	Input to the modulator accepts digital data in NRZ form. When ITXD is low, the modulator output frequency is 2200Hz. When ITXD is high, the modulator output frequency is 1200Hz.
IXTL	Oscillator Input	Input to the internal oscillator must be connected to a parallel mode 460.8kHz ceramic resonator when using the internal oscillator or grounded when using an external 460.8kHz clock signal
OCBIAS	Comparator Bias Current	The current through this output controls the operating parameters of the internal operational amplifiers and comparators. For normal operation, OCBIAS current is set to 2.54A.
OCD	Carrier Detect Output	Output goes high when a valid input is recognized on IRXA. If the received signal is greater than the threshold specified on ICDREF for four cycles of the IRXA signal, the valid input is recognized.
ORXAF	Analog Receive Filter Output	Signal is the square wave output of the receiver high-pass filter
ORXD	Digital Receive Output (CMOS)	Signal outputs the digital receive data. When the received signal (IRXA) is 1200Hz, ORXD outputs logic high. When the received signal (IRXA) is 2200Hz, ORXD outputs logic low. ORXD is qualified internally with OCD.
OTXA	Analog Transmit Output	Output provides the trapezoidal signal controlled by ITXD. When ITXD is low, the output frequency is 2200Hz. When ITXD is high, the output frequency is 1200Hz. This output is active when INRTS is low and 0.5 V_{DC} when INRTS is high.
OXTL	Oscillator Output	Output from the internal oscillator must be connected to an external 460.8kHz clock signal or to a parallel mode 460.8kHz ceramic resonator when using the internal oscillator
TEST(12:1)	Factory Test	Factory test pins; for normal operation, tie these signals as per Table 1 and Table 2
VDD	Digital Power	Power for the digital modem circuitry
VDDA	Analog Supply Voltage	Power for the analog modem circuitry
VSS	Ground	Analog and digital ground
VSSA	Analog Ground	

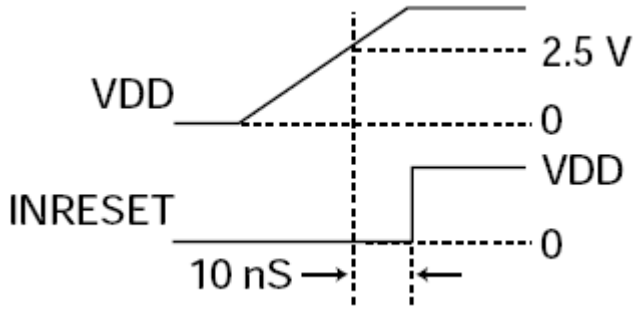


Figure 3: Reset Timing

Note:
This signal is also present on the LSI 20C15. It is labeled as Test6. The 20C15 data sheet mentions the reset function of this pin but does not emphasize its use to reset the chip. Reliable operation of the modem requires a hardware reset as shown in Figure 3. This is true for the AMIS 12197-503 and 12197-504 as well as the LSI 20C15.

4.0 Functional Description

The A5191HRT is a functional equivalent of the SYM20C15 HART Modem. It contains a transmit data modulator and signal shaper, carrier detect circuitry, analog receiver and demodulator circuitry and an oscillator, as shown in Figure 4.

The internal HART modem modulates the transmit-signal and demodulates the receive signal. The transmit-signal shaper enables the A5191HRT to transmit a HART compliant signal. The carrier is detected by comparing the receiver filter output with the difference between two external voltage references. The analog receive circuitry band-pass filters the received signal for input to the modem and the carrier detect circuitry. The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

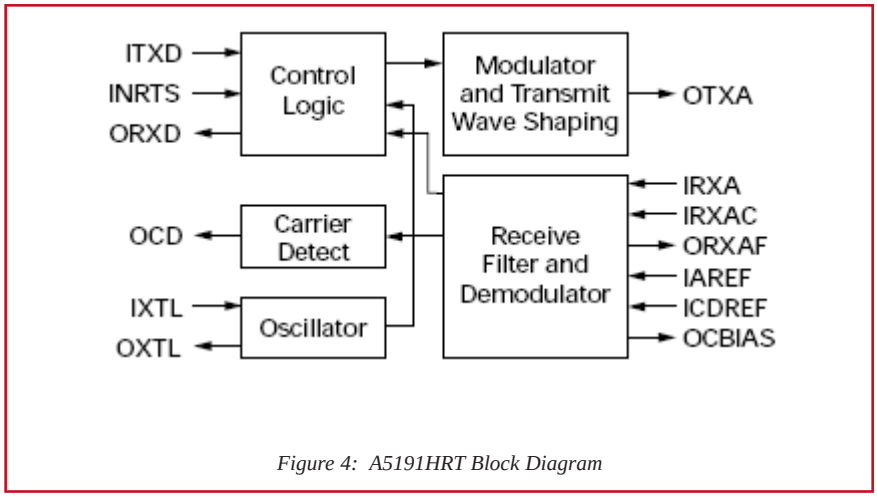


Figure 4: A5191HRT Block Diagram

4.1 A5191HRT Logic

The modem consists of a modulator and demodulator. The modem uses shift frequencies of nominally 1200Hz (for a 1) and 220Hz (for a 0). The bit rate is 1200 bits/second.

4.1.1 Modulator

The modulator accepts digital data in NRZ form at the ITXD input and generates the FSK modulated signal at the OTXA output. INRTS must be a logic low for the modulator to be active.

4.1.2 Demodulator

The demodulator accepts an FSK signal at the IRXA input and reproduces the original modulating signal at the ORXD output. The nominal bit rate is 1200 bits per second. Figure 5 illustrates the demodulation process.

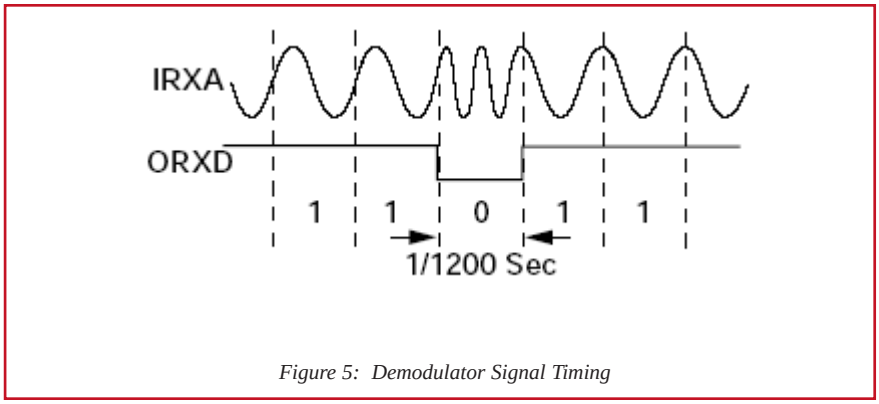


Figure 5: Demodulator Signal Timing

The output of the demodulator is qualified with the carrier detect signal (OCD), therefore, only IRXA signals large enough to be detected (100mV$_{p-p}$ typically) by the carrier detect circuit produce received serial data at ORXD.

Maximum demodulator jitter is 12 percent of one bit given input frequencies within HART specifications, a clock frequency of 460.8kHz (±1.0 percent) and zero input (IRXA) asymmetry.

4.2 Transmit-Signal Shaper

The transmit-signal shaper generates a HART compliant FSK modulated signal at OTXA. Figure 6 and Figure 7 show the transmit-signal forms of the A5191HRT.

For IAREF = 1.235 V$_{DC}$, OTXA will have a voltage swing from approximately 0.25 to 0.75 V$_{DC}$.

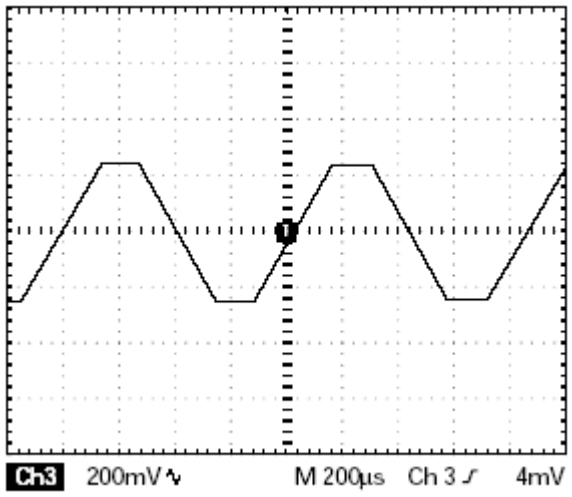


Figure 6: OTXA Waveform (1200Hz)

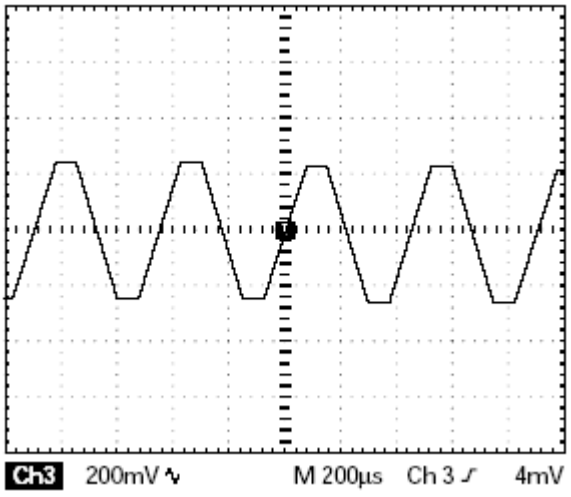


Figure 7: OTXA Waveform (2200Hz)

4.3 Carrier Detect Circuitry

The carrier detect comparator shown in Figure 8 generates logic low output if the IRXAC voltage is below ICDREF. The comparator output is fed into a carrier detect block (see Figure 4). The carrier detect block drives the carrier detect output pin OCD high if INRTS is high and four consecutive pulses out of the comparator have arrived. OCD stays high as long as INRTS is high and the next comparator pulse is received in less than 2.5ms. Once OCD goes inactive, it takes four consecutive pulses out of the comparator to assert OCD again. Four consecutive pulses amount to 3.33ms when the received signal is 1200Hz and to 1.82ms when the received signal is 2200HZ.

4.4 Analog Receiver Circuitry

4.4.1 Voltage References

The A5191HRT requires two voltage references, IAREF and ICDREF.

IAREF sets the dc operating point of the internal operational amplifiers and comparators. A 1.235 V$_{DC}$ reference (Analog Devices AD589) is suitable as IAREF.

The level at which OCD (carrier detect) becomes active is determined by the dc voltage difference (ICDREF - IAREF). Selecting a voltage difference of 0.08 V$_{DC}$ will set the carrier detect to a nominal 100 mV$_{p-p}$.

4.4.2 Bias Current Resistor

The A5191HRT requires a bias current resistor to be connected between OCBIAS and V_{SS}. The bias current controls the operating parameters of the internal operational amplifiers and comparators.

The value of the bias current resistor is determined by the reference voltage IAREF and the following formula:

$$R_{BIAS} = \left(\frac{IAREF}{2.5\,\mu A} \right)$$

The recommended bias current resistor is 500KΩ when IAREF is equal to 1.235 V_{DC}.

In Figure 8 all external capacitor values have a tolerance of ±5 percent and the resistors have a tolerance of ±1 percent, except the 3MΩ which has a tolerance of ±5 percent. External to the A5191HRT, the filter exhibits a three-pole, high-pass filter at 624Hz and a one-pole, low-pass filter at 2500Hz. Internally, the A5191HRT has a high-pass pole at 35Hz and a low-pass pole at 90kHz. The low-pass pole can vary as much as ±30 percent. The input impedance of the entire filter is greater than 150MΩ at frequencies below 50kHz.

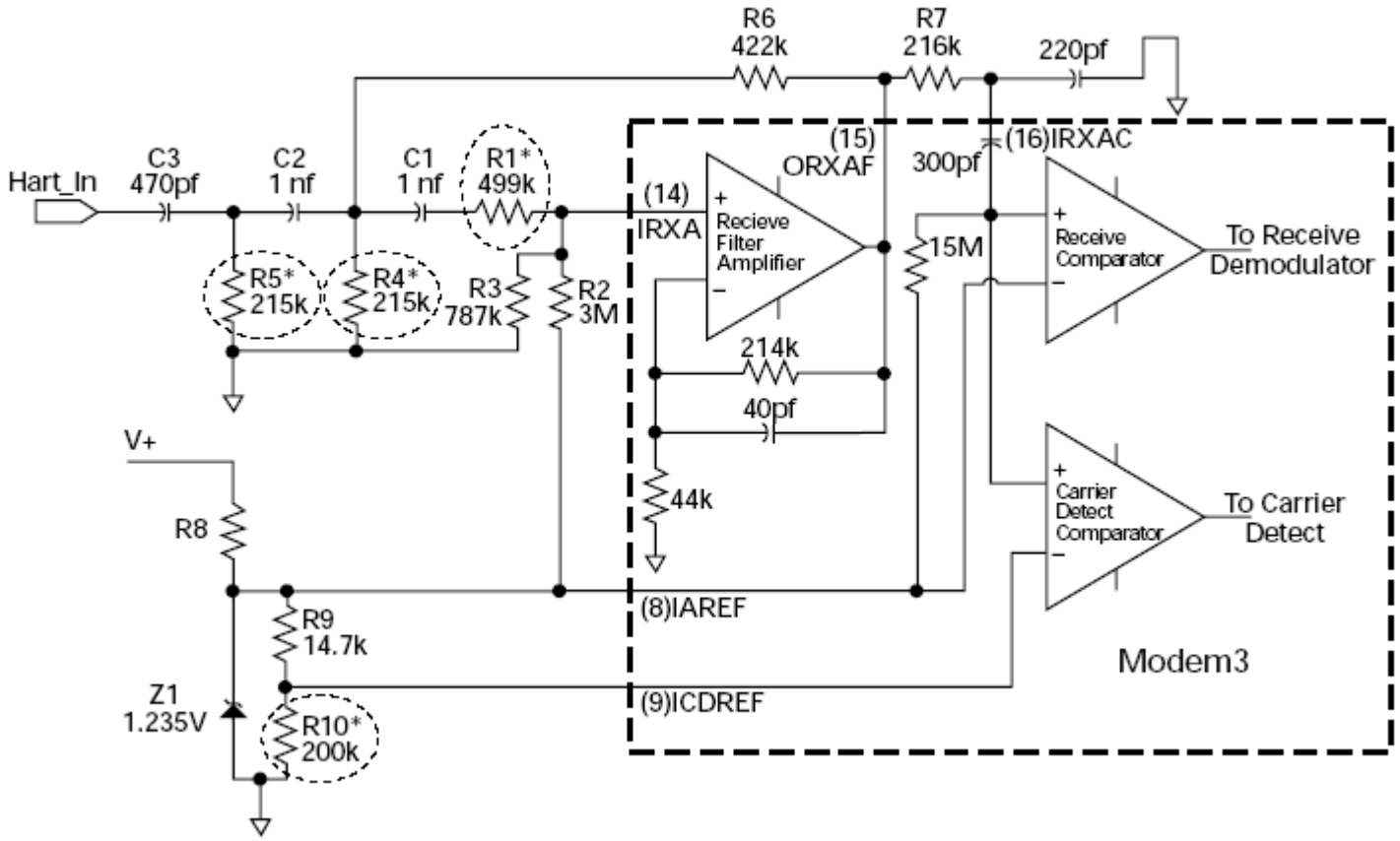


Figure 8: Receive Filter Schematic

4.5 Oscillator

The A5191HRT requires a 460.8kHz clock signal on OXTL. This can be provided by an external clock or external components may be connected to the A5191HRT internal oscillator.

4.5.1 Internal Oscillator Option

The oscillator cell will function with either a 460.8kHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between OXTL and IXTL. Figure 9 illustrates the crystal option for clock generation using a 460.8kHz (±l percent tolerance) parallel resonant crystal and two tuning capacitors. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 100pF to 470pF are used.

4.5.2 External Clock Option

It may be desirable to use an external 460.8kHz clock as shown in Figure 10 rather than the internal oscillator because of the high cost and low availability of ceramic resonators. In addition, the A5191HRT consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to OXTL and IXTL connected to V_{SS}.

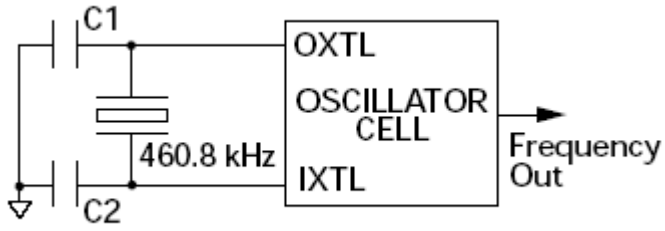


Figure 9: Crystal Oscillator

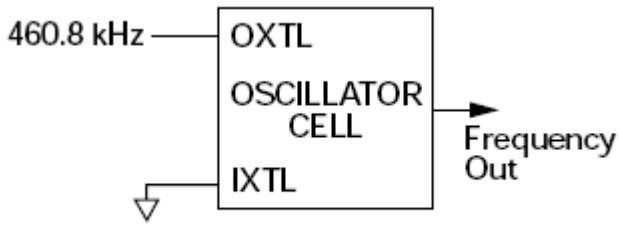


Figure 10: Oscillator with External Clock

5.0 Ordering Information

The A5191HRT is available in a 28-pin plastic leaded chip carrier (PLCC) and 32-pin low-profile quad flat pack (LQFP). Use the following part number when ordering. Contact your local sales representative for more information: www.amis.com/sales.

Table 4: Ordering Codes

Package	Package Type	Part Name	Ordering Code*
32-pin LQFP	Standard (non-Pb-free)	A5191HRTL	12197-503-XTP
28-pin PLCC	Standard (non-Pb-free)	A5191HRTP	12197-504-XTP
32-pin LQFP	Green/RoHS compliant	A5191HRTLg	12197-507-XTP
28-pin PLCC	Green/RoHS compliant	A5191HRTPg	12197-508-XTP

*The part number extension -XTP refers to the device being shipped as tape and reel. The suffix -XTD refers to shipment in tubes or tray.

6.0 Electrical Specifications

Table 5: Absolute Maximums

Symbol	Parameter	Min.	Max.	Units
T_A	Ambient	-40	+85	°C
T_S	Storage temperature	-55	150	°C
V_{DD}	Supply voltage	-0.3	6.0	V
V_{IN}, V_{OUT}	DC input,output	-0.3	V_{DD}+0.3	V
T_L	Re-flow solder profile		per IPC/JEDEC J-STD-020C	°C

Cautions:

1. CMOS devices are damaged by high-energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating. Stresses above absolute maximum ratings may result in damage to the device.
2. Remove power before insertion or removal of this device.

Table 6: DC Characteristics

V_{DD} = 3.0V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C

Symbol	Parameter	VDD	Min.	Typ.	Max.	Units
V_{IL}	Input voltage, low	3.0 - 5.5			0.3*V_{DD}	V
V_{IH}	Input voltage	3.0 - 5.5	0.7*V_{DD}			V
V_{OL}	Output voltage, low (I_{OL} = 0.67mA)	3.0 - 5.5			0.4	V
V_{OH}	Output voltage, high (I_{OH} = -0.67mA)	3.0 - 5.5	2.4			V
C_{IN}	Input capacitance Analog input IRXA Digital input			2.9 25 3.5		pF
$I_{IL/IH}$	Input leakage current				±500	nA
I_{OLL}	Output leakage current				±10	µA
I_{DD}	Power supply current (RBIAS = 500kΩ, IAREF = 1.235V)	3.3 5.0		330 400	450 600	µA
IAREF	Analog reference	3.3 5.0	1.2	1.235 2.5	2.6	V
ICDREF*	Carrier detect reference (IAREF - 0.08V)			1.15		V
OCBIAS	Comparator bias current (RBIAS = 500kΩ, IAREF = 1.235V)			2.5		µA

*The HART specification requires carrier detect (OCD) to be active between 80 and 120 mV_{p-p}. Setting ICDREF at IAREF - 0.08 V_{DC} will set the carrier detect to a nominal 100 mV_{p-p}.

Table 7: AC Characteristics

V_{DD} = 3.0V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C

Pin Name	Description	Min.	Typ.	Max.	Units
IRXA	Receive analog input Leakage current Frequency - mark (logic 1) Frequency - space (logic 0)	 1190 2180	 1200 2200	 ±150 1210 2220	 nA Hz Hz
ORXAF	Output of the high-pass filter Slew rate Gain bandwidth (GBW) Voltage range	 150 0.15	 0.025 	 V_{DD} - 0.15	 V/µs kHz V/µs
IRXAC	Carrier detect and receive filter input Leakage current	 	 	 ±500	 nA
OTXA	Modulator output Frequency - mark (logic 1) Frequency - space (logic 0) Amplitude (IAREF 1.235V) Slope Loading (IAREF = 1.235V)	 30	 1196.9 2194.3 500 2.79 	 	 Hz Hz mV_{P-P} mV/µs kΩ
ORXD	Receive digital output Rise/fall time	 20	 	 	 ns
OCD	Carrier detect output Rise/fall time	 20	 	 	 ns

The modular output frequencies are proportional to the input clock frequency (460.8kHz).

Table 8: Modem Characteristics

V_{DD} = 3.0V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C

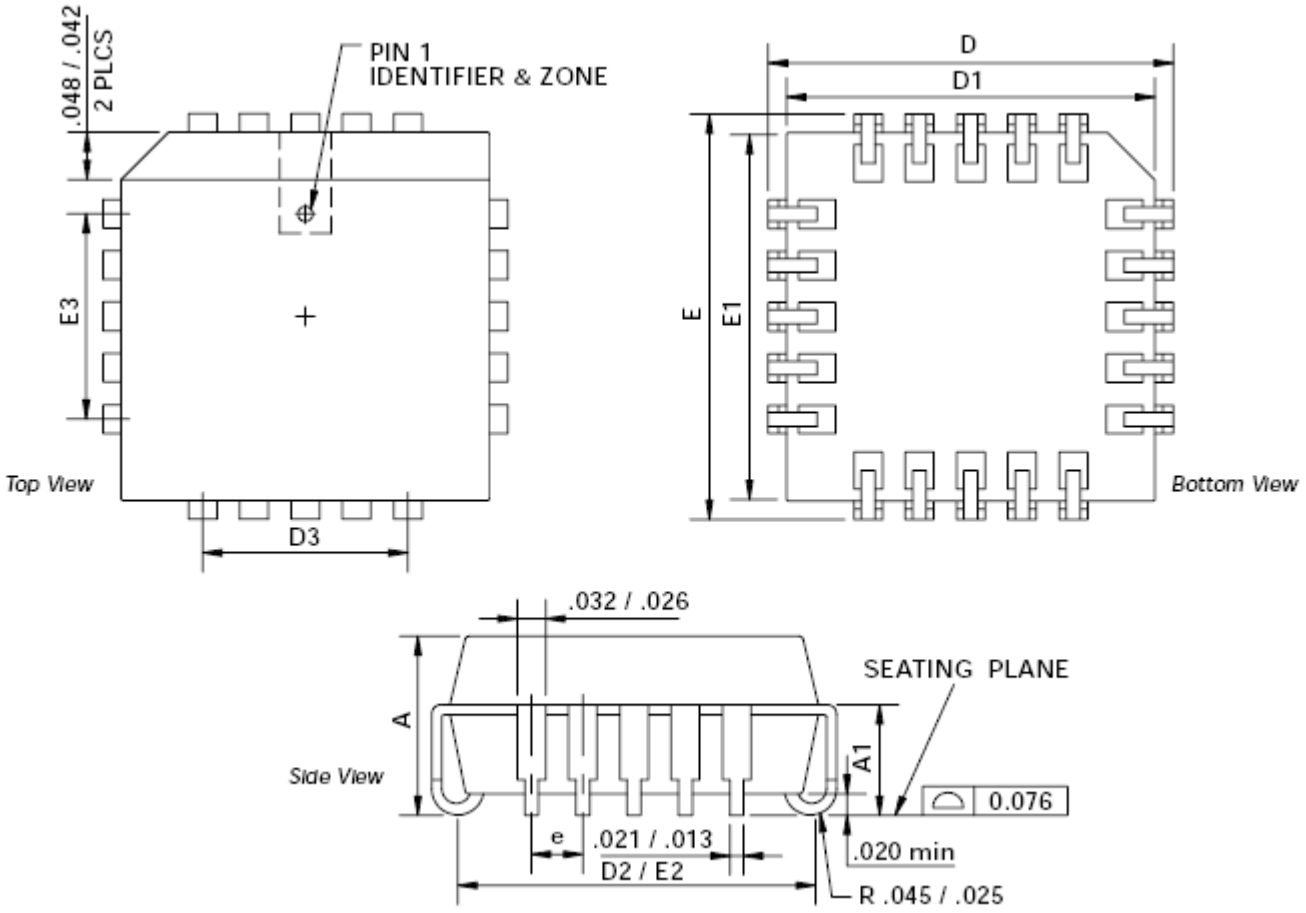
Parameter	Min.	Typ.	Max.	Units
Demodulator Jitter Conditions 1. Input frequencies at 1200Hz ± 10Hz, 2200Hz ± 20Hz 2. Clock frequency of 460.8kHz ± 0.1% 3. Input (HLXA) asymmetry, 0			12	% of 1 bit

Table 9: Ceramic Resonator - External Clock Specifications

V_{DD} = 3.0V to 5.5V, V_{SS} = 0V, T_A = -40°C to +85°C

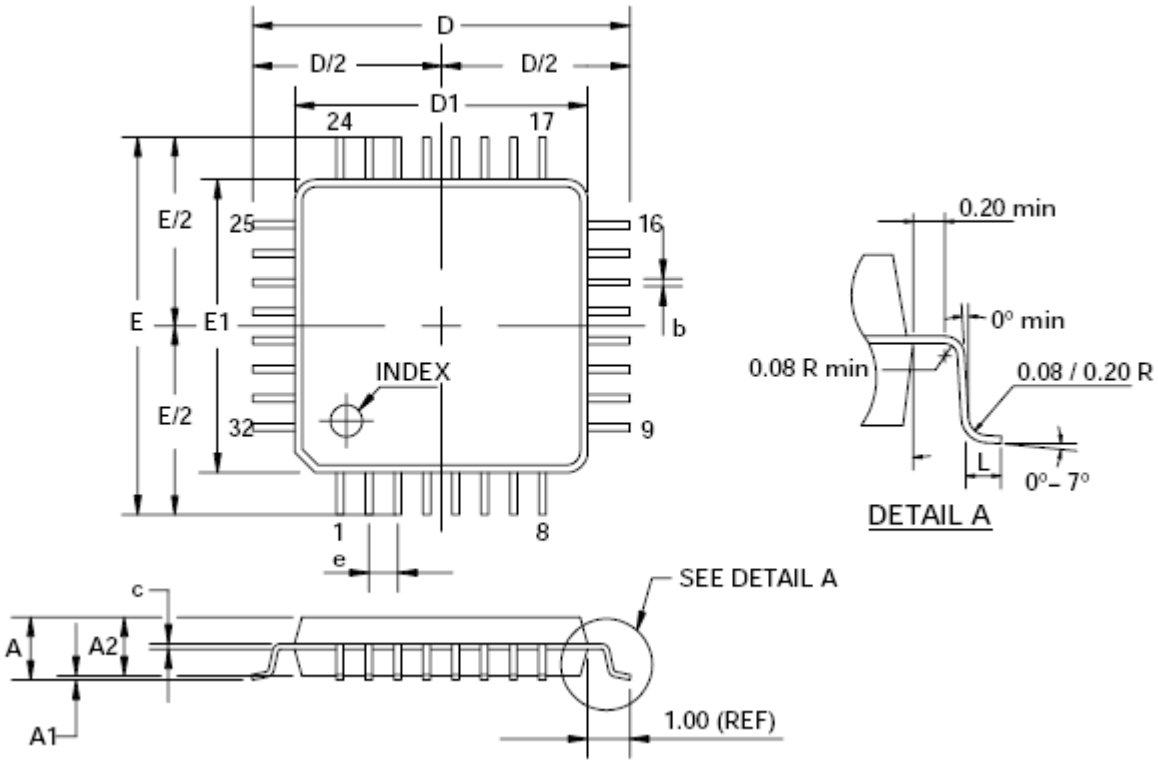
Parameter	Min.	Typ.	Max.	Units
Resonator Tolerance Frequency	 460.8	 	 1.0 	 % kHz
External Clock frequency Duty cycle Amplitude	 456.2 40	 460.8 50 V_{OH} - V_{OL}	 465.4 60	 kHz % V

7.0 Mechanical Specifications



Symbol	Min.	Nom.	Max.
A	.165	.172	.180
A1	.099	.101	.110
D	.485	.490	.495
D1	.450	.452	.455
D2	.390	.420	.430
D3		.300 REF	
E	.485	.490	.495
E1	.450	.452	.455
E2	.390	.420	.430
E3		.300 REF	
e		.050 BSC	

Figure 11: 28 Lead PLCC



Symbol	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D		9.00 BSC	
D/2		4.50 BSC	
D1		7.00 BSC	
E		9.00 BSC	
E/2		4.50 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
e		0.80 BSC	
b	0.30	0.37	0.45
c	0.09	-	0.20
ccc	-	-	0.10
ddd	-	-	0.20

Figure 12: 32 Lead LQFP